**20EC41O2-DSP PROCESSORS & ARCHITECTURE**

| **Course Category:** | Program Elective | **Credits:** | 3 |
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| **Course Type:** | Theory | **Lecture -Tutorial-Practical:** | 2-2-0 |
| **Prerequisite:** | Basics of Signals and systems | **Sessional Evaluation:****External Evaluation:****Total Marks:** | 4060100 |

| **Course****Objectives** | Students undergoing this course are expected: |
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| 1. To teach the basic concepts DSP
2. To educate the students about types Computational errors
3. To educate the students to develop & design architectures for programmable DSP
4. To show how to Write programming to dsp devices
5. To educate the students about implementation of FFT algorithms
6. To educate the students about interfacing
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| **Course Outcomes** | Upon successful completion of the course , the students will be able to: |
| CO1 | Understand various types of LTI systems |
| CO2 | Understand computational accuracy in DSP applications |
| CO3 | Develop the develop & design architectures for programmable DSP |
| CO4 | Develop the programming to DSP devices |
| CO5 | Develop the FFT algorithms |
| CO6 | Design different I/O interfacings  |
| **Course****Content** |  **UNIT –I****INTRODUCTION TO DIGITAL SIGNAL PROCESING**: Linear Time-Invariant systems, Digital filters, Decimation and interpolation, Analysis and Design tool for DSP Systems MATLAB, DSP using MATLAB.**UNIT-II****COMPUTATIONAL ACCURACY IN DSP IMPLEMENTATIONS:** Number formats for signals and coefficients in DSP systems, Dynamic Range and Precision, Sources of error in DSP implementations, A/D Conversion errors, DSP Computational errors, D/A Conversion Errors, Compensating filter. |
| **Course****Content** | **UNIT-III****ARCHITECTURES FOR PROGRAMMABLE DSP DEVICES-I:** Basic Architectural features, DSP Computational Building Blocks, Bus Architecture and Memory, Data Addressing Capabilities, Address Generation Unit, Programmability and Program Execution, Speed Issues, Features for External interfacing, Commercial Digital signal-processing Devices, **UNIT-IV****ARCHITECTURES FOR PROGRAMMABLE DSP DEVICES-II:**Data Addressing modes, Memory space, instructions, Program Control of TMS320C54XX Processors, and Programming On-Chip Peripherals, Interrupts, Pipeline Operation of TMS320C54XX Processors.**UNIT- V****IMPLEMENTATIONS OF BASIC DSP & FFT ALGORITHMS:** The Q-notation, FIR Filters, IIR Filters, Interpolation Filters, Decimation Filters, PID Controller, Adaptive Filters, 2-D Signal Processing. An FFT Algorithm for DFT Computation, A Butterfly Computation, Overflow and scaling, Bit-Reversed index generation, An 8-Point FFT implementation on the TMS320C54XX, Computation of the signal spectrum.**UNIT- VI****INTERFACING MEMORY AND I/O PERIPHERALS TO PROGRAMMABLE DSP DEVICES:** Memory space organization, External bus interfacing signals, Memory interface, Parallel I/O interface, Programmed I/O, Interrupts and I/O, Direct memory access (DMA). A Multichannel buffered serial port (McBSP), McBSP Programming, a CODEC interface circuit, CODEC programming, A CODEC-DSP interface example. |
| **Text Books and Reference Books** | **TEXT BOOKS:**1. Digital Signal Processing – Avtar Singh and S. Srinivasan, Thomson Publications, 2004.2. DSP Processor Fundamentals, Architectures & Features – Lapsley et al.S. Chand & CO, 2000.**REFERENCE BOOKS:** 1. Digital Signal Processors, Architecture, Programming and Applications-B.VenkataRamani and M. Bhaskar, TMH, 2004.
2. Digital Signal Processing – Jonatham Stein, John Wiley, 2005.
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| **E-Resources** | 1. http://www.nptel.ac.in.2. http:/www.ebookee.com/dsp processors and architectures. |